

TSMC-02-428



November 17, 2003

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/644,322 08/20/03

Chung-Shi Chiang et al.

A NEW CHARACTERIZATION METHODOLOGY
FOR THE THIN GATE OXIDE DEVICE

Grp. Art Unit: _____

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
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mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on November 21, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

SBAR 11/21/03

There are quite a few publications that discuss gate current related issues. Some of there publications include:

- 1) "Hole Injection SiO₂ Breakdown Model for Very Low Voltage Lifetime Extrapolation," by K.F. Schuegraf et al., IEEE Trans. Elec. Dev., Vol. 41(5), pp. 761-767, May 1994.
- 2) "Modeling Gate and Substrate Currents due to Conduction- and Valence-Band Electron and Hole Tunneling," by W.C. Lee et al., 2000 Symposium on VLSI Tech., PP. 198-199, 2000.
- 3) "1.5 nm Direct-Tunneling Gate Oxide Si MOSFET's by Hisayo Sakaki Momose et al., IEEE Trans. Elec. Dev., Vol. 43(8), pp. 1233-1242, Aug. 1996.
- 4) "BSIM4 Gate Leakage Model Including Source-Drain Partition," by K.M. Cao et al., 2000 IEDM, pp. 35.3.1 to 35.3.4.
- 5) Operation and Modeling of the MOS Transistor, by Yannis P. Tsividis, McGraw-Hill Book Company, NY, Copyright 1988, pp. 88-99.

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U.S. Patent 6,246,973 to Sekine, "Modeling Method of MOSFET," discusses modeling channel width.

U.S. Patent 6,378,109 to Young et al., "Method of Simulation for Gate Oxide Integrity Check on an Entire IC," teaches a method to simulate a gate oxide integrity check.

U.S. Patent 6,391,668 to Chacon et al., "Method of Determining a Trap Density of a Semiconductor/Oxide Interface by a Contactless Charge Technique," discloses a method of determining trap density from measured current.

Sincerely,

A handwritten signature in black ink, appearing to read 'SBA', is written over the printed name.

Stephen B. Ackerman,
Reg. No. 37761

Doc No: (Cp-0100)

Tsmc-02-428

Application Number

10/644, 322

Applicant

Applicant Chung-Shi Chiang et al.

Filing Date

Filing Date 08/20/03

Group Art Unit

EXAMINER
INITIAL

DOCUMENT NUMBER

DATE

NAME

CLUB

WDC:LMH

PLUMB DATE
IF APPROPRIATE

OTPE JG173
OV 2 4 2003
TRADEMARK OFFICE

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Sekine

703

4

8/12/99

6	3	7	8	1	0	9	4	23	02
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Young et al.

716

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6/30/00

63916685/21/02

Chacon et al.

438

17

5/1/00

DOCUMENT NUMBER

DATE _____

COUNTRY

CLASS

SUBCLASS

Translation

YES

25

OTHER DOCUMENTS (Including Author, Title, Date, Portion or Pages, Etc.)

"Hole Injection SiO₂ Breakdown Model for Very Low Voltage Lifetime Extrapolation", K.F. Schwarzgraf et al., IEEE Trans. Elec. Dev. Vol. 41(5) pp. 761-767 May 1994

"modeling Gate and Substrate Currents due to Conduction - and - Valence-Band Electron and Hole Tunneling" W.C. Lee et al. 2000 Symposium VLSI Tech., pp.198-199 2000

"1.5nm Direct-Tunneling Gate Oxide Si MOSFET's, Hisayo Sakaki Momose et al.,
IEEE Trans. Elec. Dev., Vol. 43(8) pp.1233-1242, Aug. 1996.

*BSIM4 Gate Leakage Model Including Source-Drain Partition, K.M.Cao et al., 2000 IEDM pp. 35.3.1 - 35.3.4.

Operation and Modeling of the mos Transistor, Yannis P. Tsividis,
McGraw Hill Book Co., NY, Copyright 1988, pp. 88-99.

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.